An SoC Design and Fabrication Hands-On Educational Course Within One Week Using Structured ASIC

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Why is semiconductor education difficult ?

- Recently in Japan, there has been increased investment in the semiconductor industry, such as TSMC(JASM), Micron, and Rapidus.
- However, this causes a shortage of talent.
- **Few Students Aspire to Enter the Semiconductor Field**
  - One major reason is the lack of hands-on experience in semiconductor education. .
  - Semiconductor chip fabrication experiments requires
    - The high costs and time required.
    - Extensive knowledge, including electronic circuits, CAD tools, and fabrication processes.
- **There is a strong need for student lab programs**
  - Only with basic circuit knowledge
  - Affordable cost
  - A short period of time.

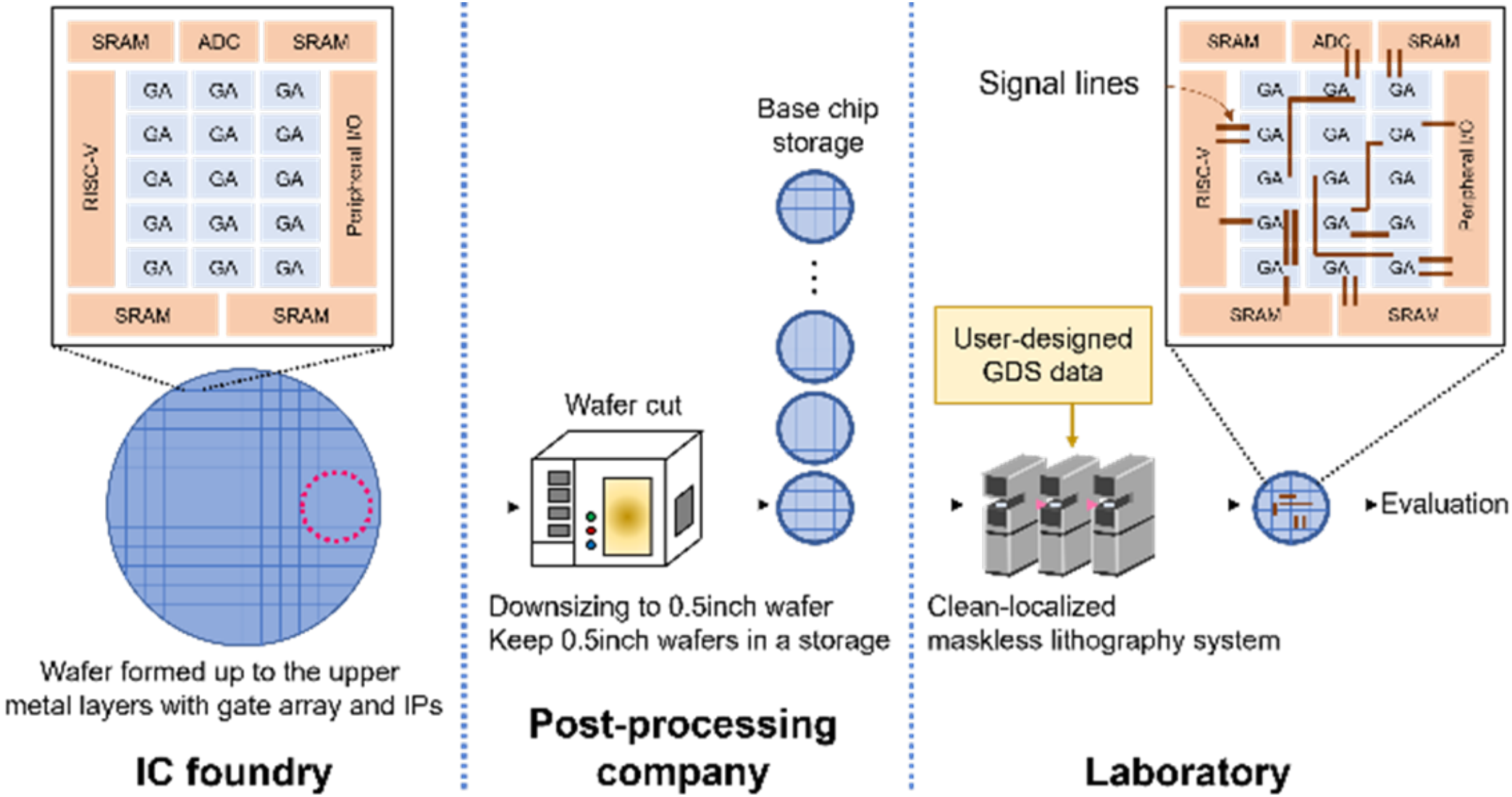
MEXT(Ministry of Education) initiated to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

To promote the formation of core academic centers for R&D and human resource development with the aim of creating innovative semiconductor LSI that will play an important role in achieving a carbon neutral 2050 and digital society, as well as ensuring economic security.

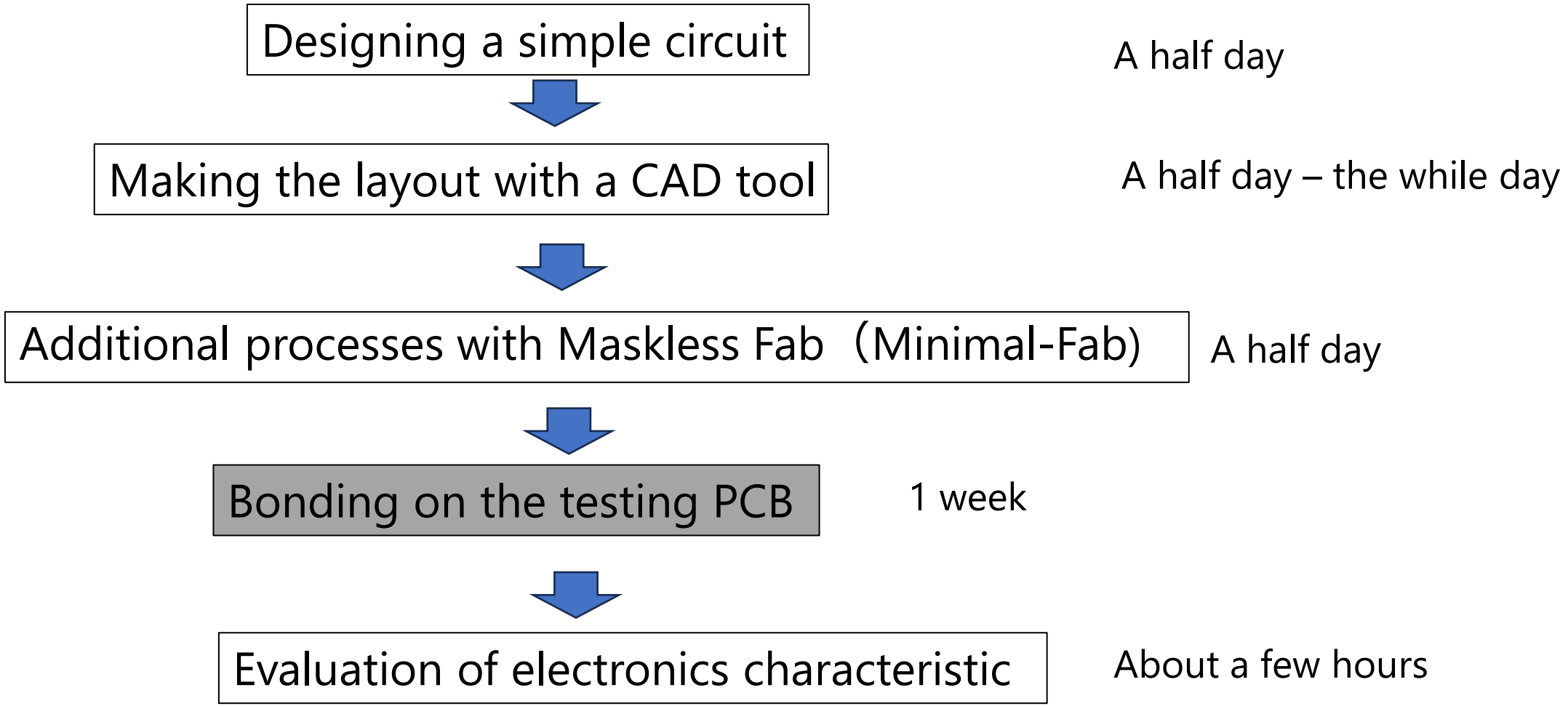
- "Agile-X Democratization Base of Innovative Semiconductor Tech", Univ. of Tokyo
- "Green-niX Res. And Education Base", Titech
- "Spintronics X Semiconductor Res. Hub", Tohoku Univ.

• Agile-X platform for TAT: 1/10, Cost: 1/10
• x10 LSI designers and make LSI democratize

Agile-X enables quick and low-cost chip development



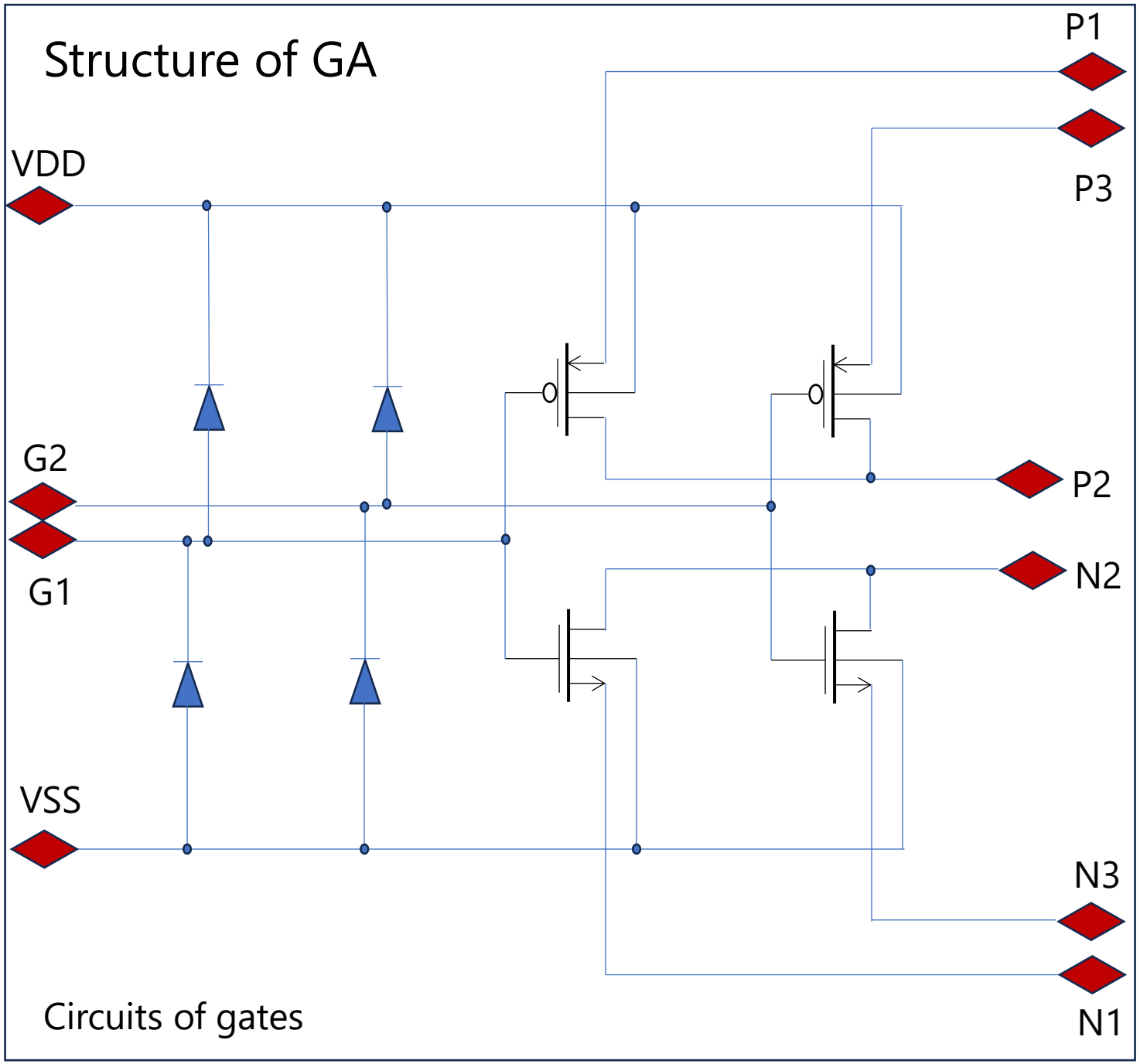
Agile-X platform enables a quick student lab.



Considerations

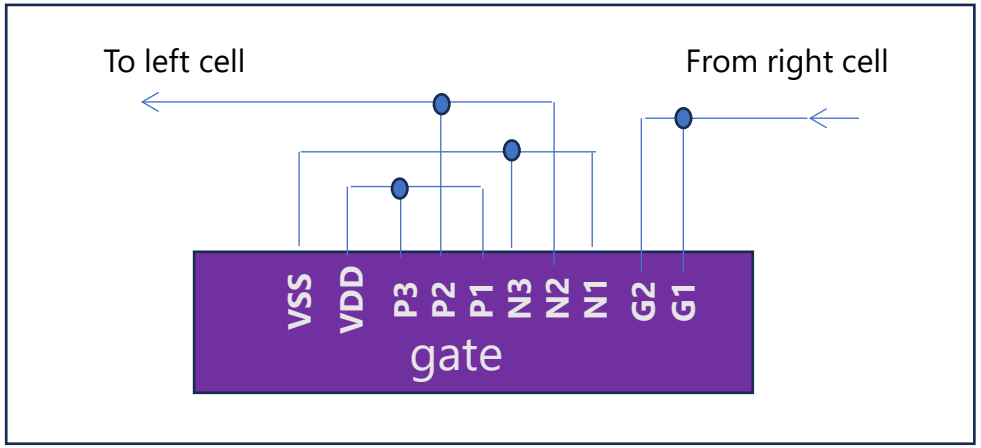
- Use a simple circuit in the GA part
  - 61-stage ring oscillator
  - Easy to understand with basic knowledge on electronics
  - Easy to verify
  - Small number of pins
- Layout with Virtuoso
  - all-in-one layout tool including DRC and LVS
  - Easy to make wires
  - LEVIS is used for confirmation of the layout
- Students need NDA

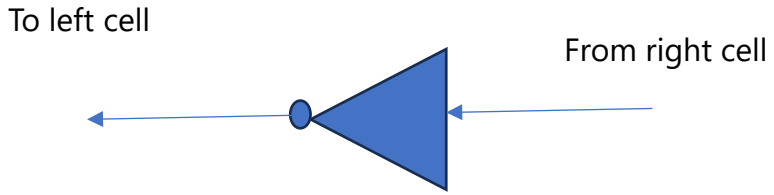
Structure of GA



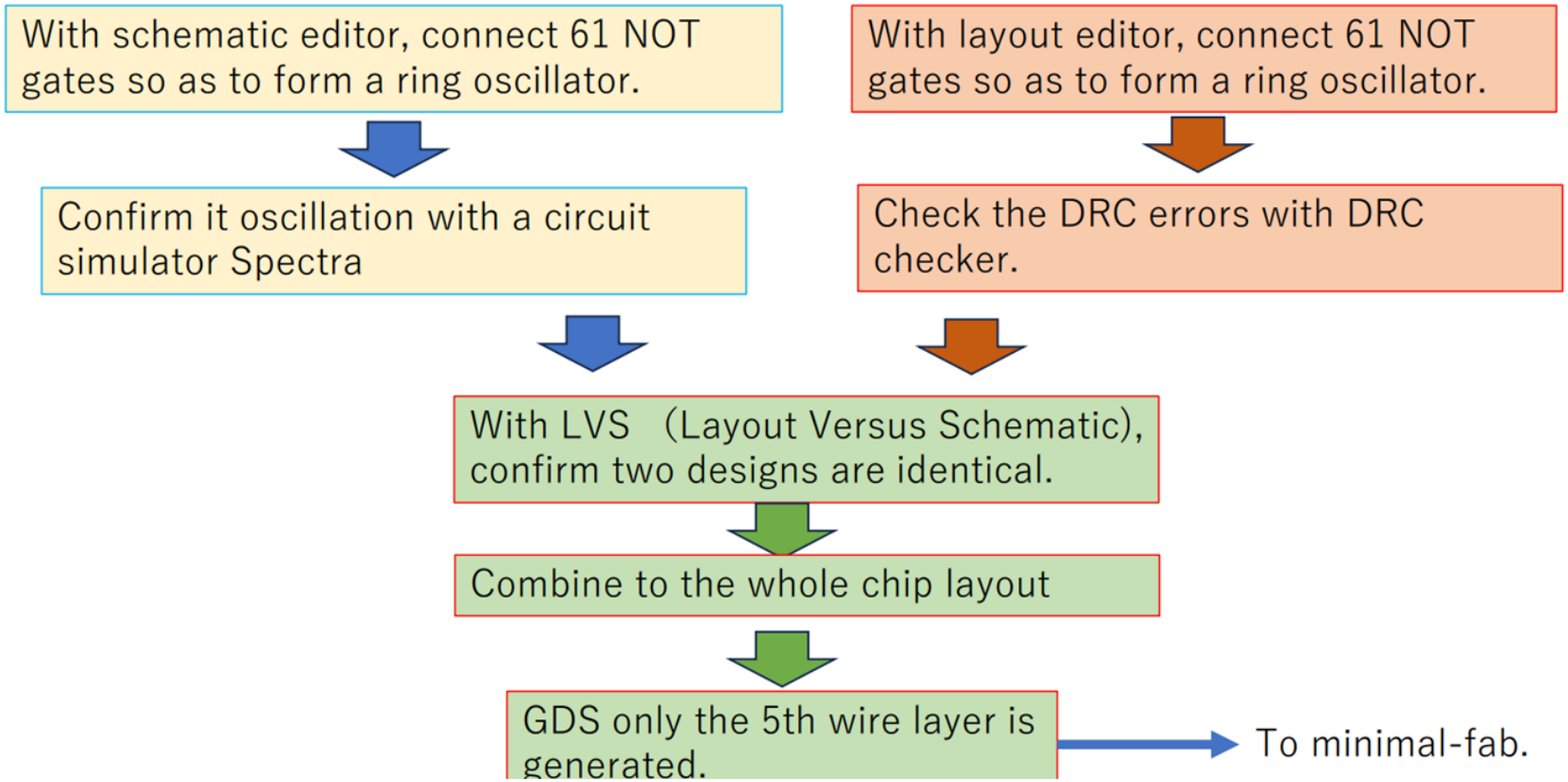
Circuits of gates

NOT gate is formed with the 5th layer wires

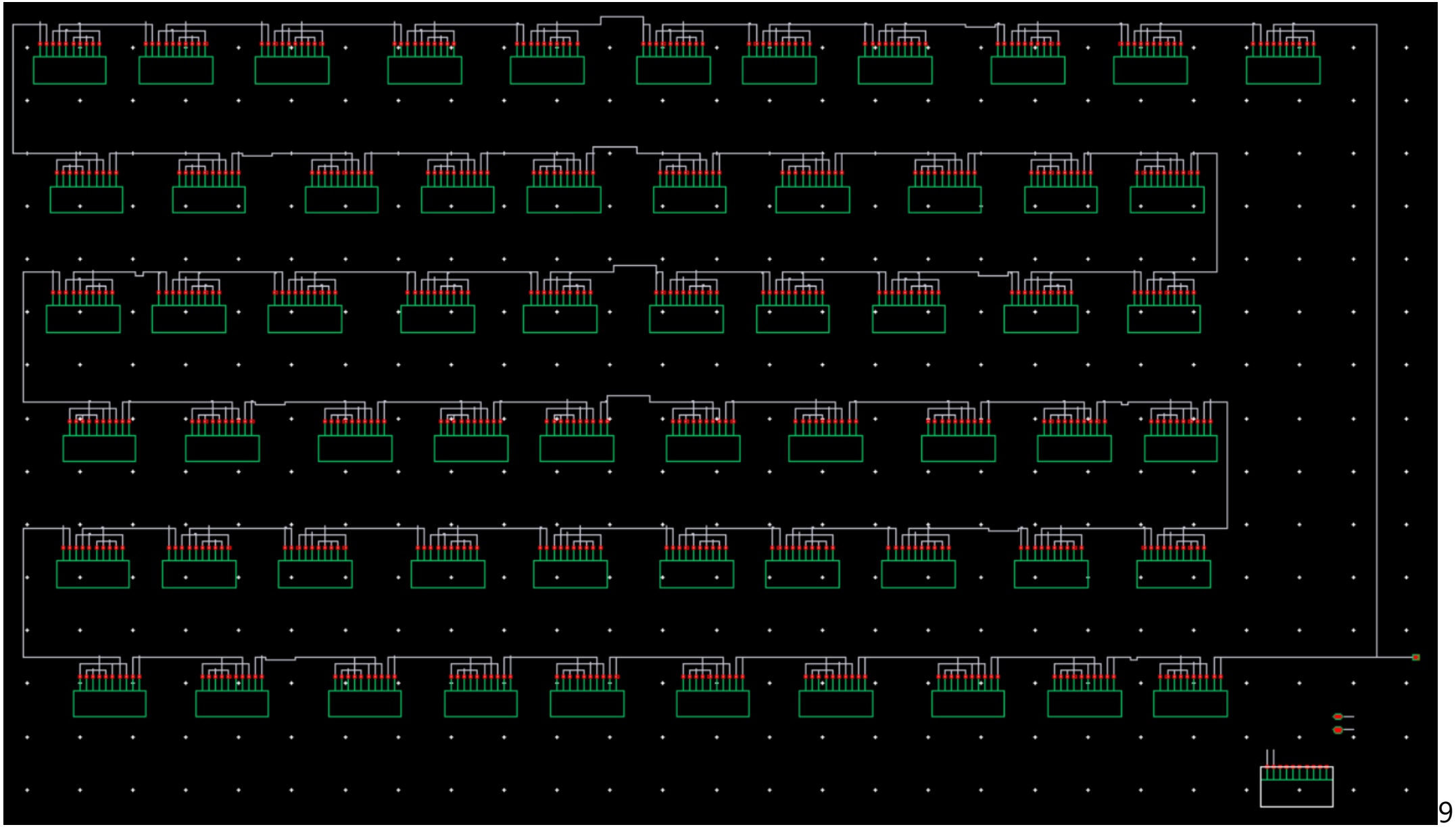




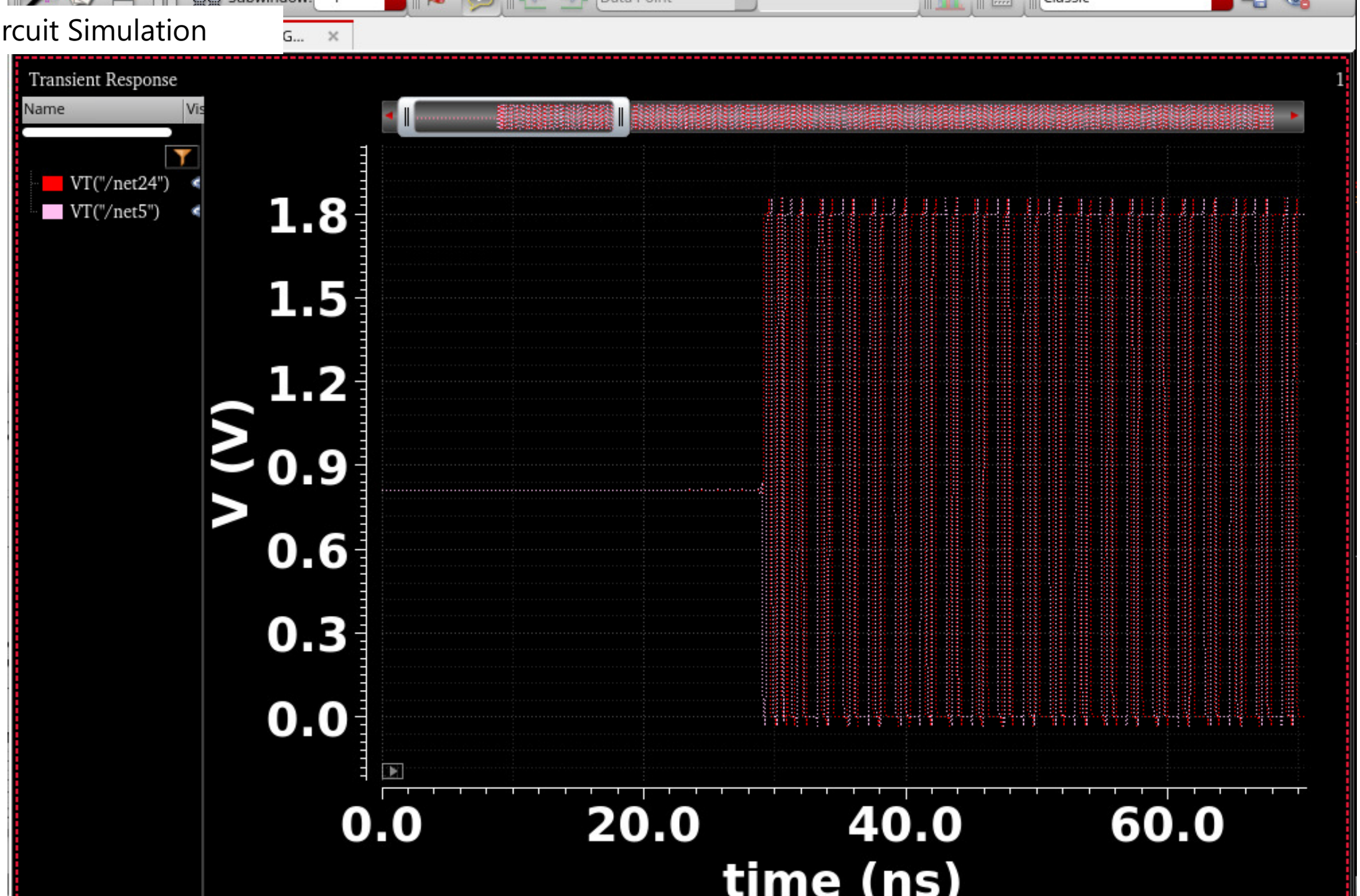
Design flow of the student lab.



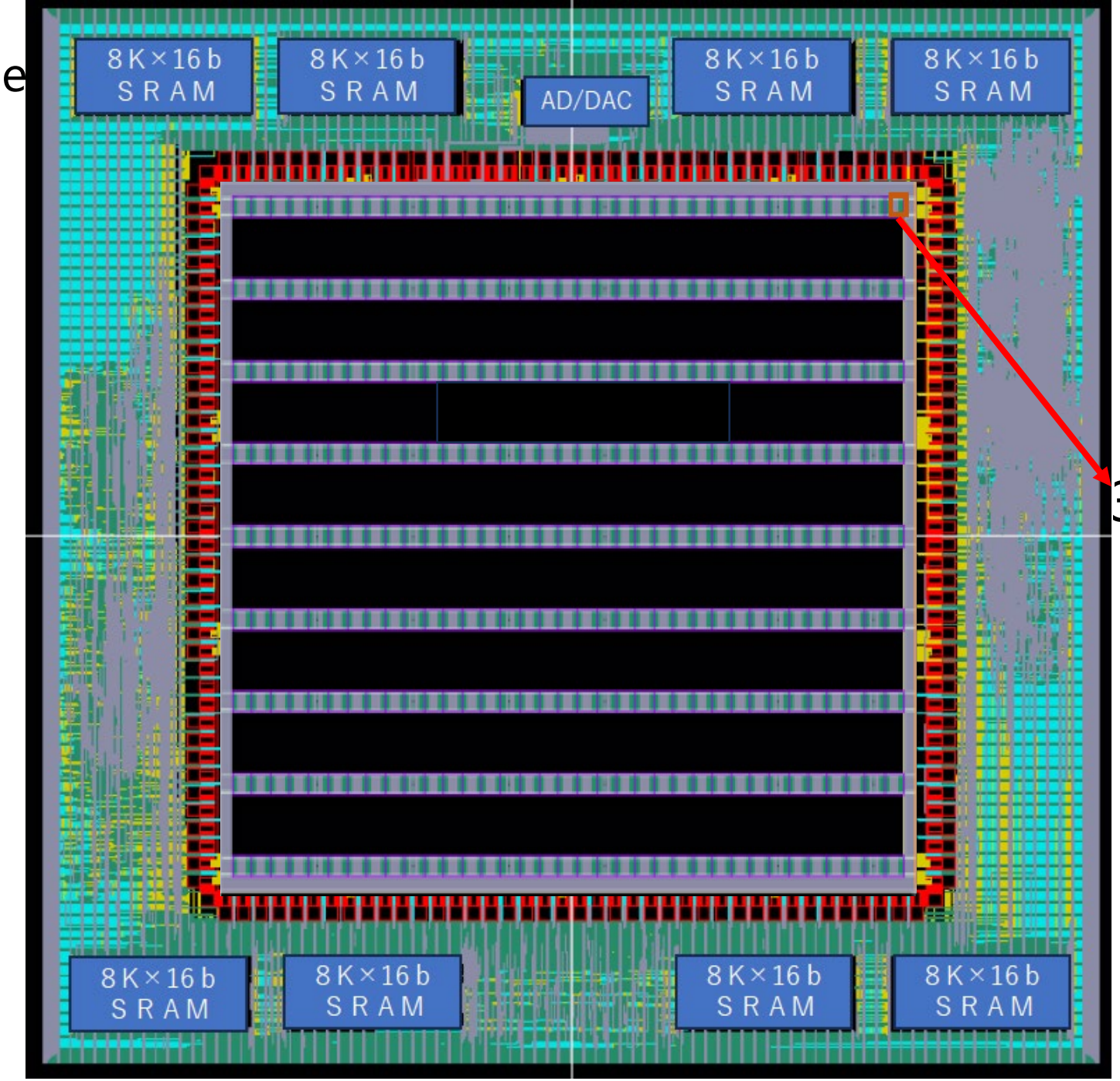
61-stage oscillator circuit　Virtuoso circuit editor



Electronics Circuit Simulation

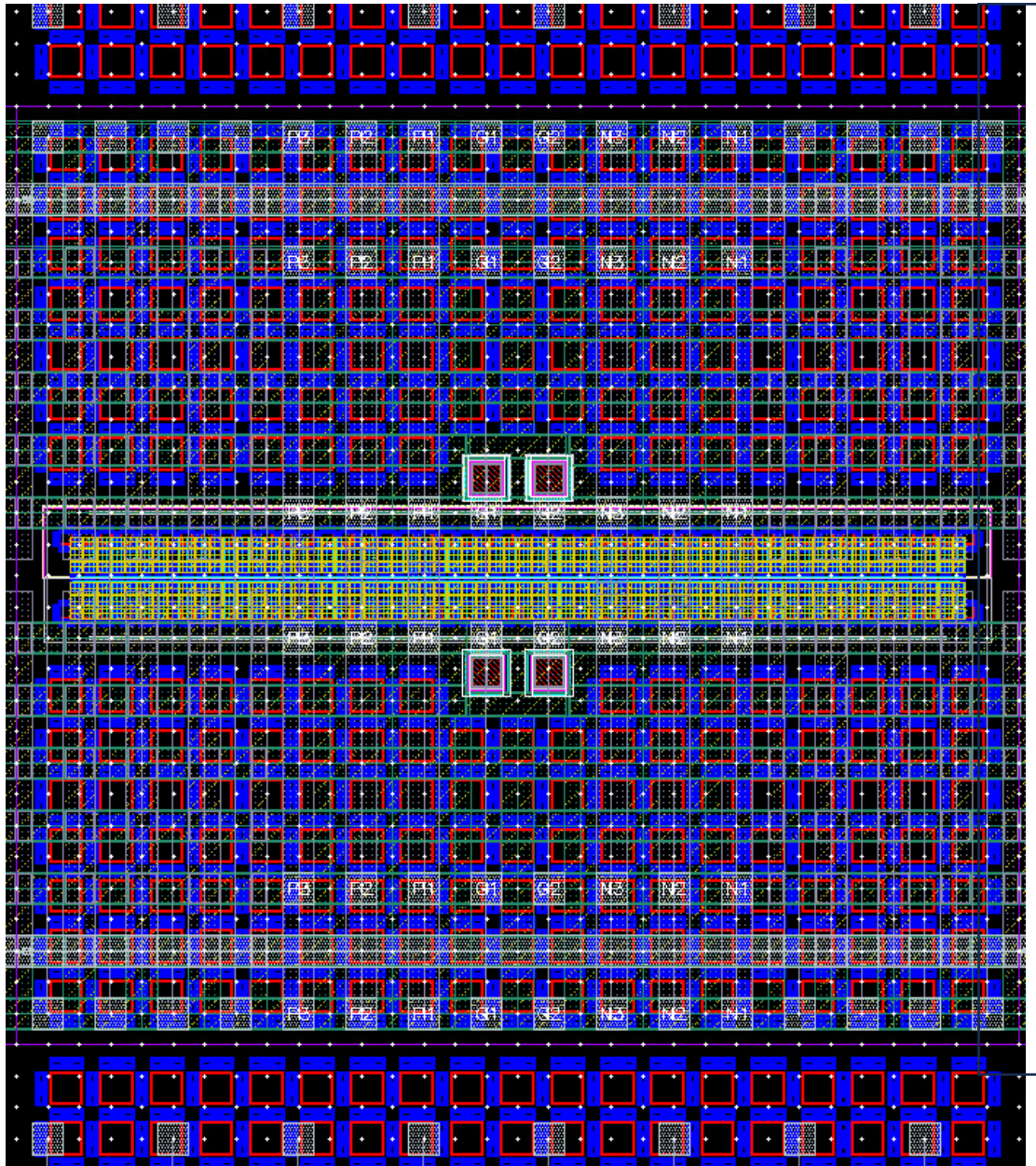


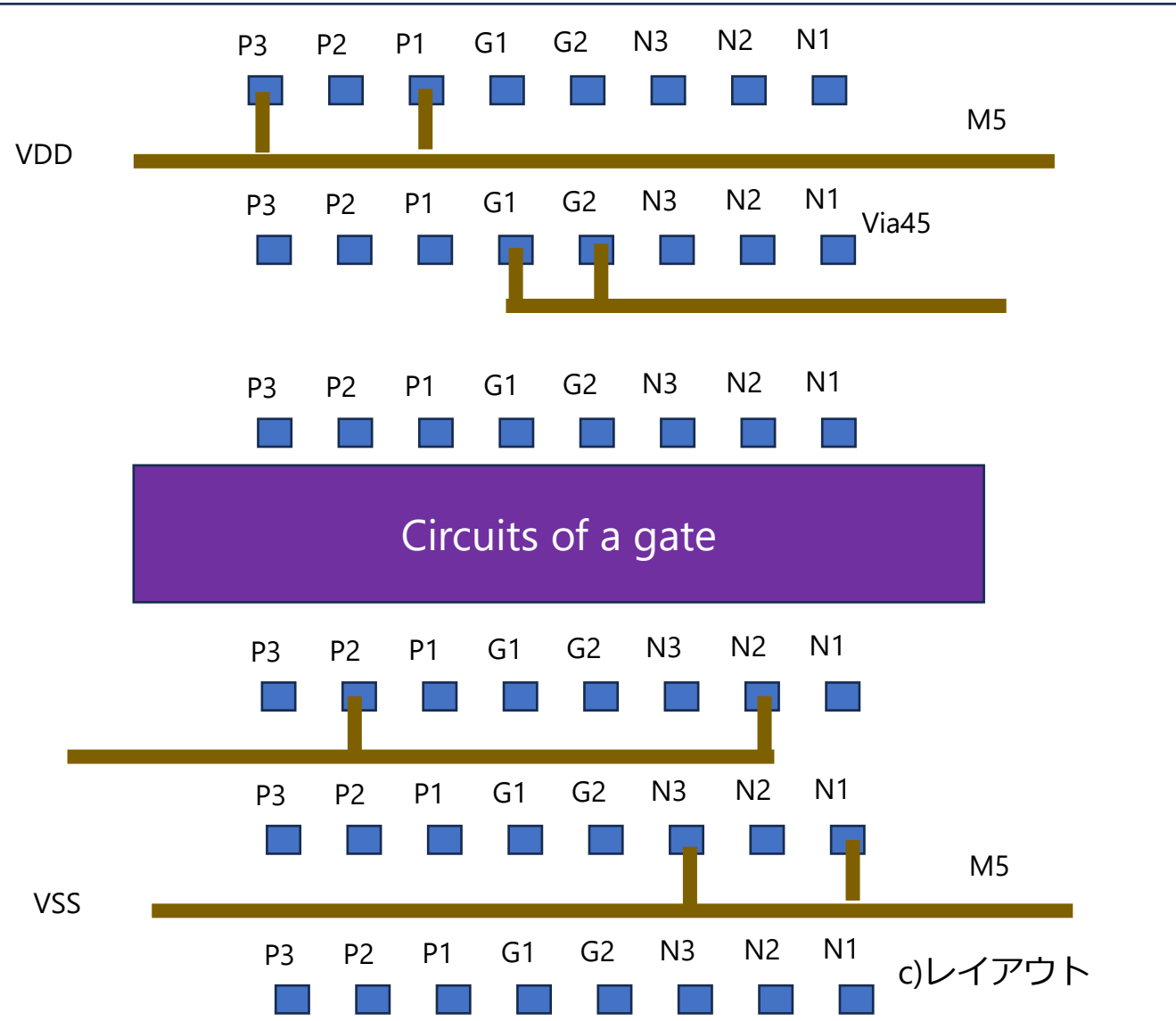
Layout of the Chip



34 gates in a row

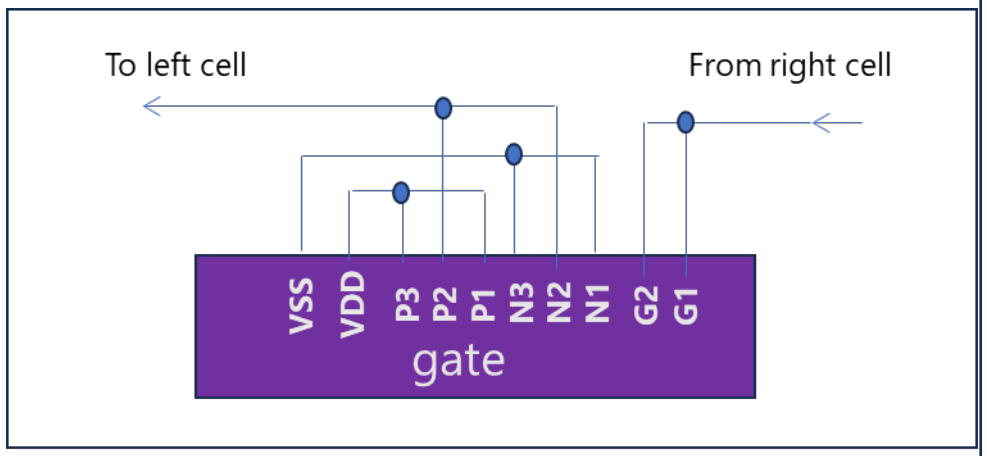
Layout for ring-oscillator

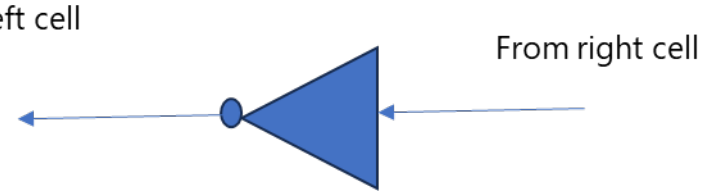


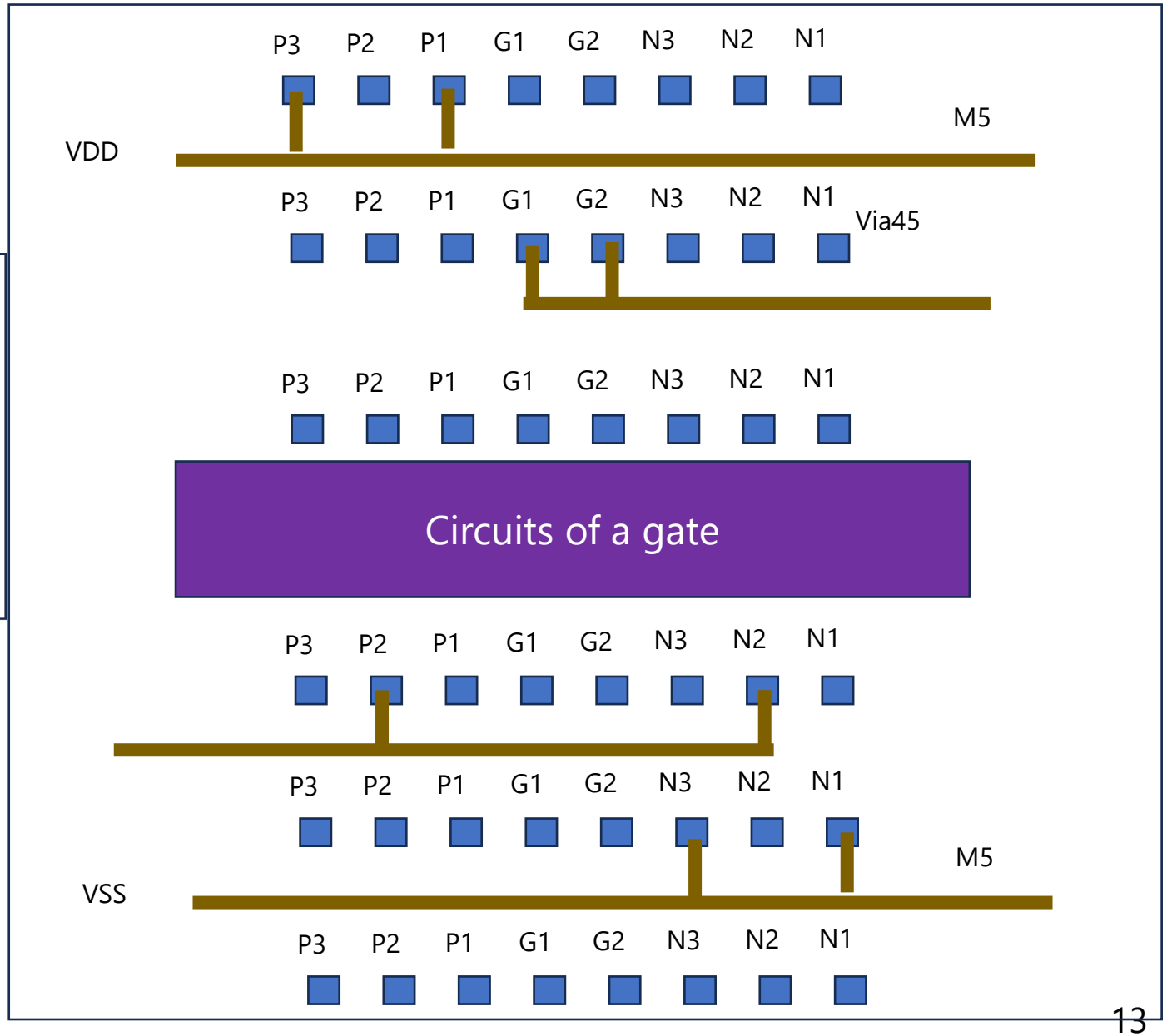


c)レイアウト

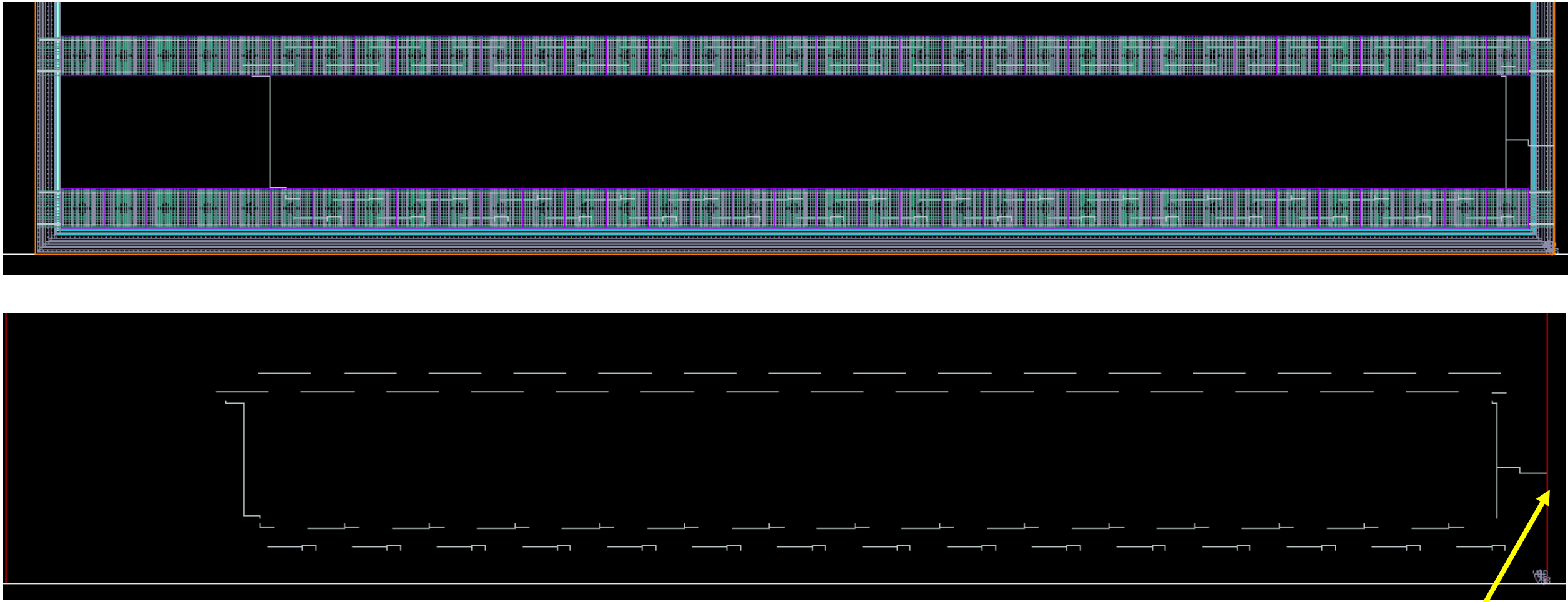
Connection of the 5th metal layer for a not gate







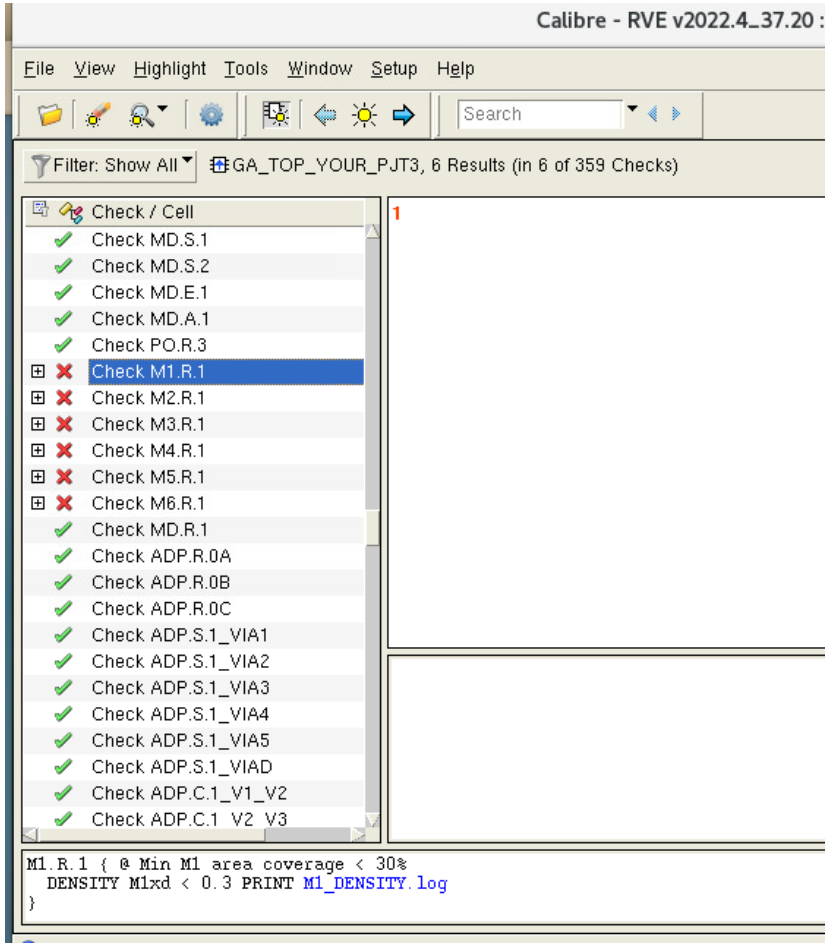
Example of the layout　30 gates (Lower) + 31 gates (Upper)



Connect to labeled PAD
ga_out[1] is used here.

DRC check　Virtuoso embedded Calibre is used.

- OK if green ✓ is shown.
- Density errors can be ignored.
- If there is no error, the layout is OK.

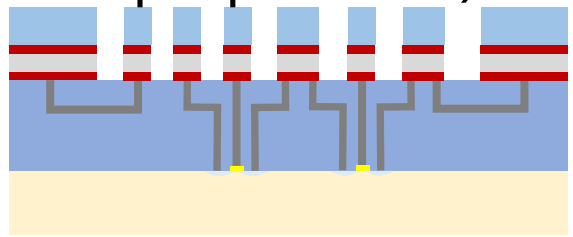


Virtuoso embedded LVS is used.
Circuits used for the simulation and the layout are compared.

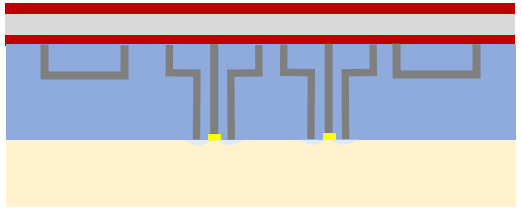
```
                ##################################################
                ##                                              ##
                ##        C A L I B R E   S Y S T E M           ##
                ##                                              ##
                ##           L V S   R E P O R T                ##
                ##                                              ##
                ##################################################



REPORT FILE NAME:         GA_TOP_YOUR_PJT3.lvs.report
LAYOUT NAME:              GA_TOP_YOUR_PJT3.sp ('GA_TOP_YOUR_PJT3')
SOURCE NAME:              GA_TOP_YOUR_PJT3.src.net ('GA_TOP_YOUR_PJT3')
RULE FILE:                _calibre.lvs_
CREATION TIME:            Mon Jul  8 17:52:50 2024
CURRENT DIRECTORY:        /home/usr/hunga/try
USER NAME:                hunga
CALIBRE VERSION:          v2022.4_37.20    Fri Dec 2 17:41:02 PST 2022



                        OVERALL COMPARISON RESULTS



                     #       ###################       _   _  |
                   #         #                 #       *   *
                 #   #       #     CORRECT     #         |
                  # #        #                 #       \___/
                   #         ###################


  Warning:  Unbalanced smashed mosfets were matched.
  Warning:  Ambiguity points were found and resolved arbitrarily.
  Warning:  LVS property resolution maximum exceeded.


*********************************************************************************************************
```

Processes on Minimal-Fab

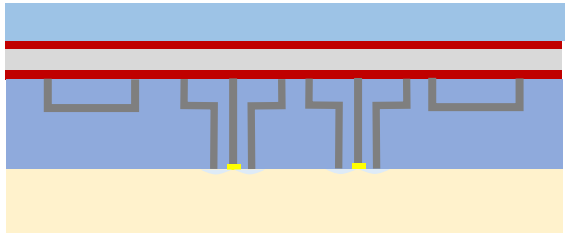
Dry Etcher
(under preparation)



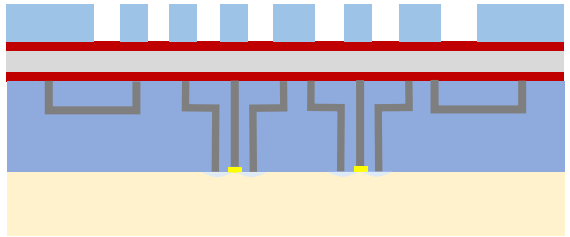
Base Chip



Spattering, Coater

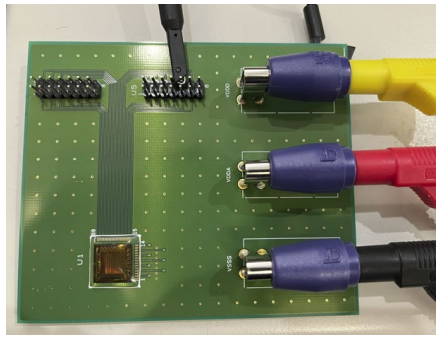


Maskless exposure, TEOS PE-CDV Development Acetone cleaner

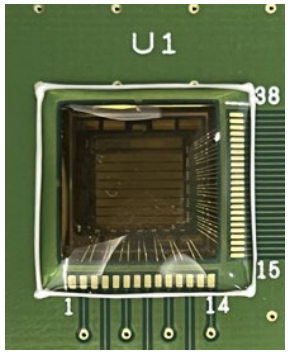


Circuits evaluation

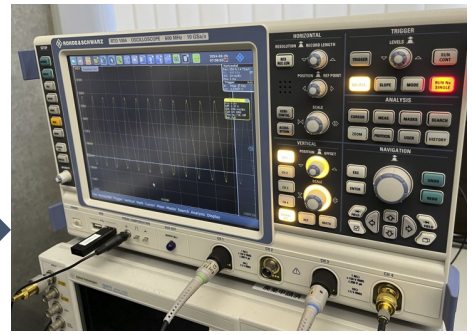
Direct bonding to the Print Circuit Board for skipping the package stage.



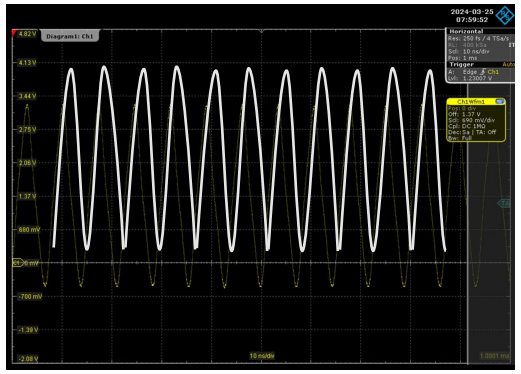
PCB



Chip



Oscilloscope
RTO1004



Evaluation of the frequency

Students solder terminals and pins.

Comparison of Cost and Total Process time

	Full mask wafer	MPW Shuttle	Our Agile-X
Cost amortization	No	By 20 designs	By 140designs per wafer By 100 base wafer
IPs	RISC-V CPU with peripheral IO		
Wafer cost	400	20	2.9 USD
Mask cost	191K	9.6K	13.6 USD
IP cost	80K	80K	5.7 USD
Total cost	271K USD (1)	89.6K USD	22.2 USD (1/12252)
Total process time	~20days	~20days	~30min. (1/960)
Assumptions	Single design only. 0.18um 1P6M CMOS.	A wafer is shared with 20 designs. IPs are not shared. 0.18um 1P6M CMOS.	100 base wafer is fabricated (14K base chip) 0.18um 1P6M CMOS.

A.Kosuge, et.al. Agile-X: A Structured-ASIC Created with a Mask-less Lithography System Enabling Low-Cost and Agile Chip Fabrication IEEE Transactions on Very Large Scale Integration Systems (Accepted)

A trial in 2024

- For Six students
  whose major is not semiconductor
- Clean-room is used instead of the Minimal Fab in 2024.
- 1 day for design and 1 day for fabrication
- All designs worked well.

Experimental Lab.

Design with CAD

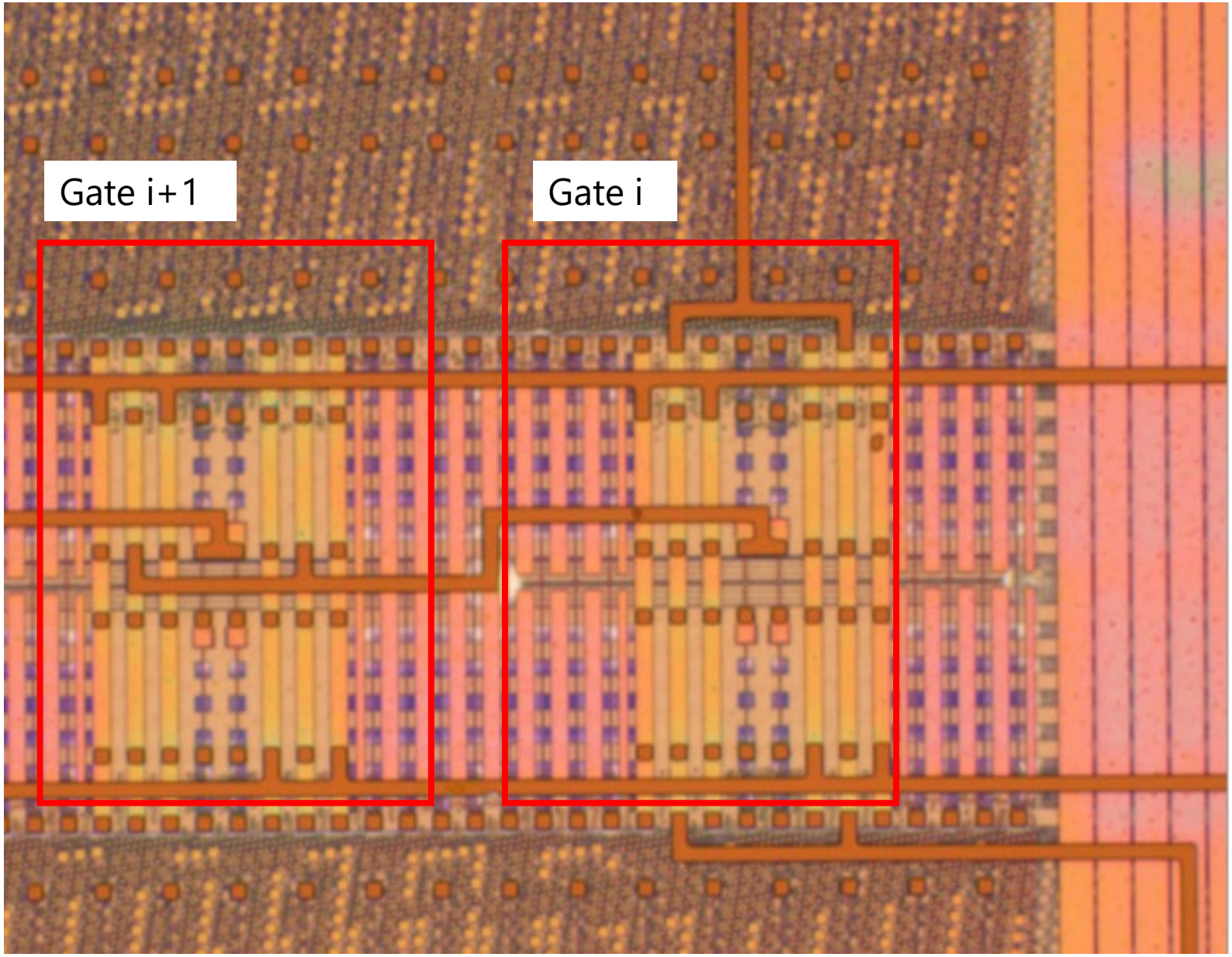
Etching

Lithography

Certification of the board

Students can select one of three chips for bonding.

Worked
at 143MHz:
delay is 0.057ns



Problems and future work

- **Students just Observe During the Manufacturing Stage**
  However, even just entering a cleanroom or handling the minimal-fab can have a significant impact on them.
- **We Currently Outsource Bonding to a Board Manufacturer.**
  - It needs a certain cost and time.
  - Bonding machine is needed, but it is handled only by a skilled engineer.
- **This Is Not a Full-Scale Semiconductor Design or Fabrication Exercise**
  - The RISC-V core and memory components are not utilized at all in the current setup.
  - However, we are currently preparing a new digital IC fabrication experiment that incorporates these peripheral components.

  → Available on this July

Thank you for your listening

- Questions?