Can the Agile-chip platform carve out a niche between ASICs and FPGAs?

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CoolChips28

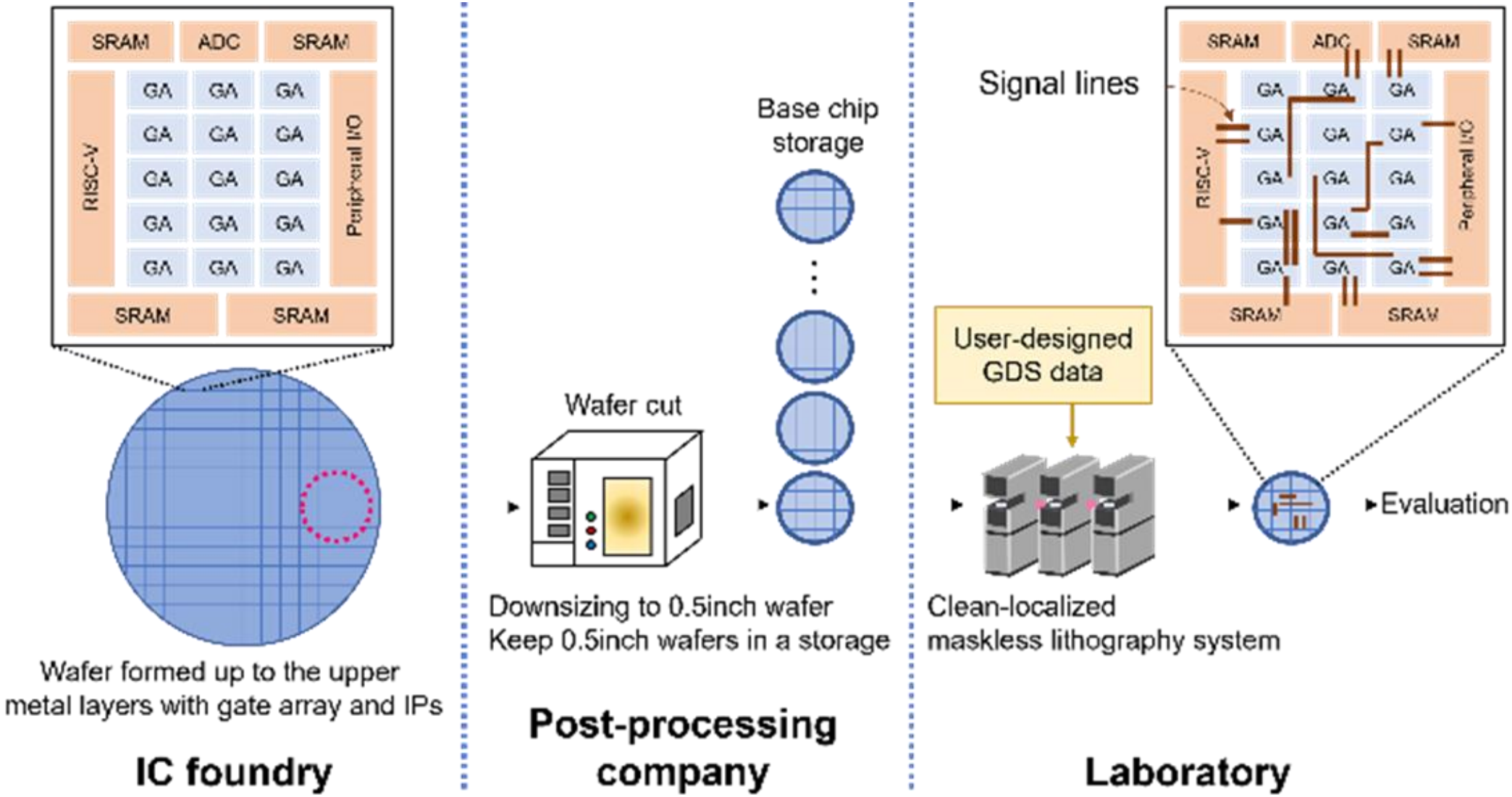
MEXT(Ministry of Education) Initiatiated to Establish Next-generation Novel Integrated Circuits Centers (X-NICS)

To promote the formation of core academic centers for R&D and human resource development that leverage Japan's strengths, with the aim of creating innovative semiconductor LSI that will play an important role in achieving a carbon neutral 2050 and digital society, as well as ensuring economic security.

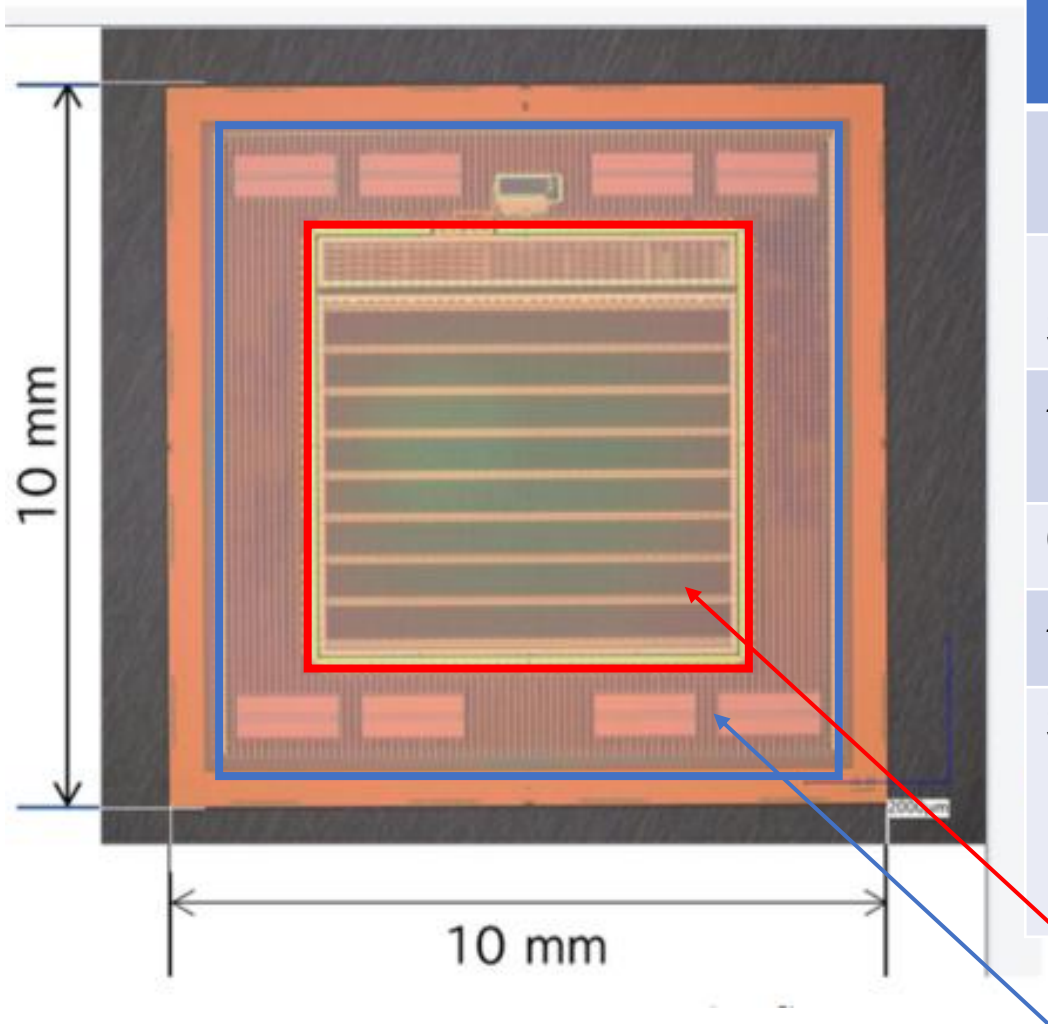
- "Agile-X Democratization Base of Innovative Semiconductor Tech", Univ. of Tokyo
- "Green-niX Res. And Education Base", Titech
- "Spintronics X Semiconductor Res. Hub", Tohoku Univ.

- Agile-X platform for TAT: 1/10, Cost: 1/10
- x10 LSI designers and make LSI democratize

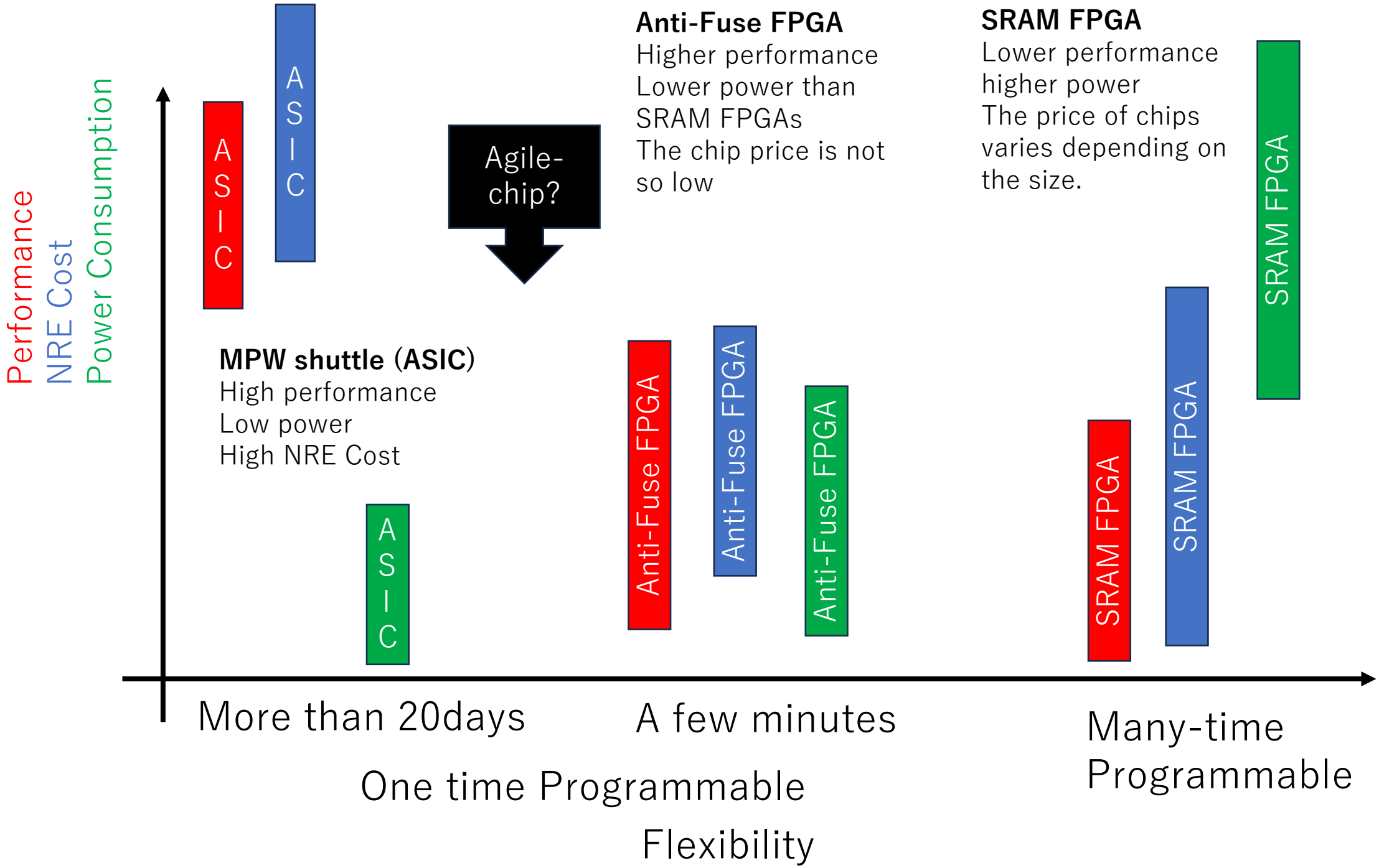
Agile-X enables quick and low-cost chip development



The current status of Agile-Chip



	Agile 1 L	Agile 2L
Process	1P6M 0.18 μ m CMOS	
Line and Space	5 μ m	1 μ m
# of layers	1 (the 5th)	2(the 5th and 6th)
GA cell size	145 × 75 μ m	34 × 28 μ m
# of GA cells	315	19680
Status	Currently available	Techniques are ready Maybe the next year

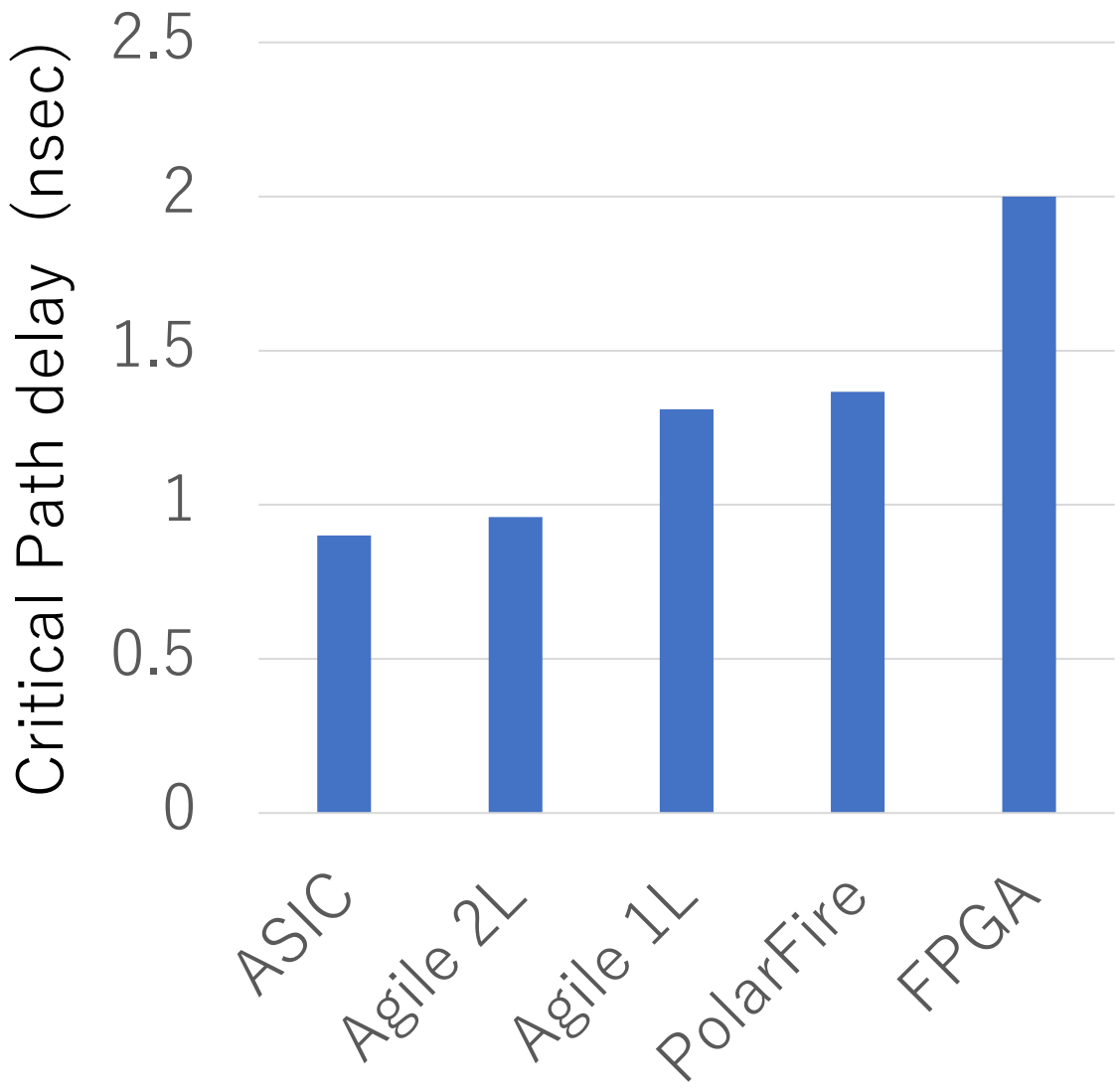

Performance
NRE Cost
Power Consumption
ASIC
ASIC
Agile-chip?
Anti-Fuse FPGA
Higher performance
Lower power than SRAM FPGAs
The chip price is not so low
SRAM FPGA
Lower performance
higher power
The price of chips varies depending on the size.
MPW shuttle (ASIC)
High performance
Low power
High NRE Cost
ASIC
Anti-Fuse FPGA
Anti-Fuse FPGA
Anti-Fuse FPGA
SRAM FPGA
SRAM FPGA
SRAM FPGA
More than 20days
A few minutes
Many-time Programmable
One time Programmable
Flexibility

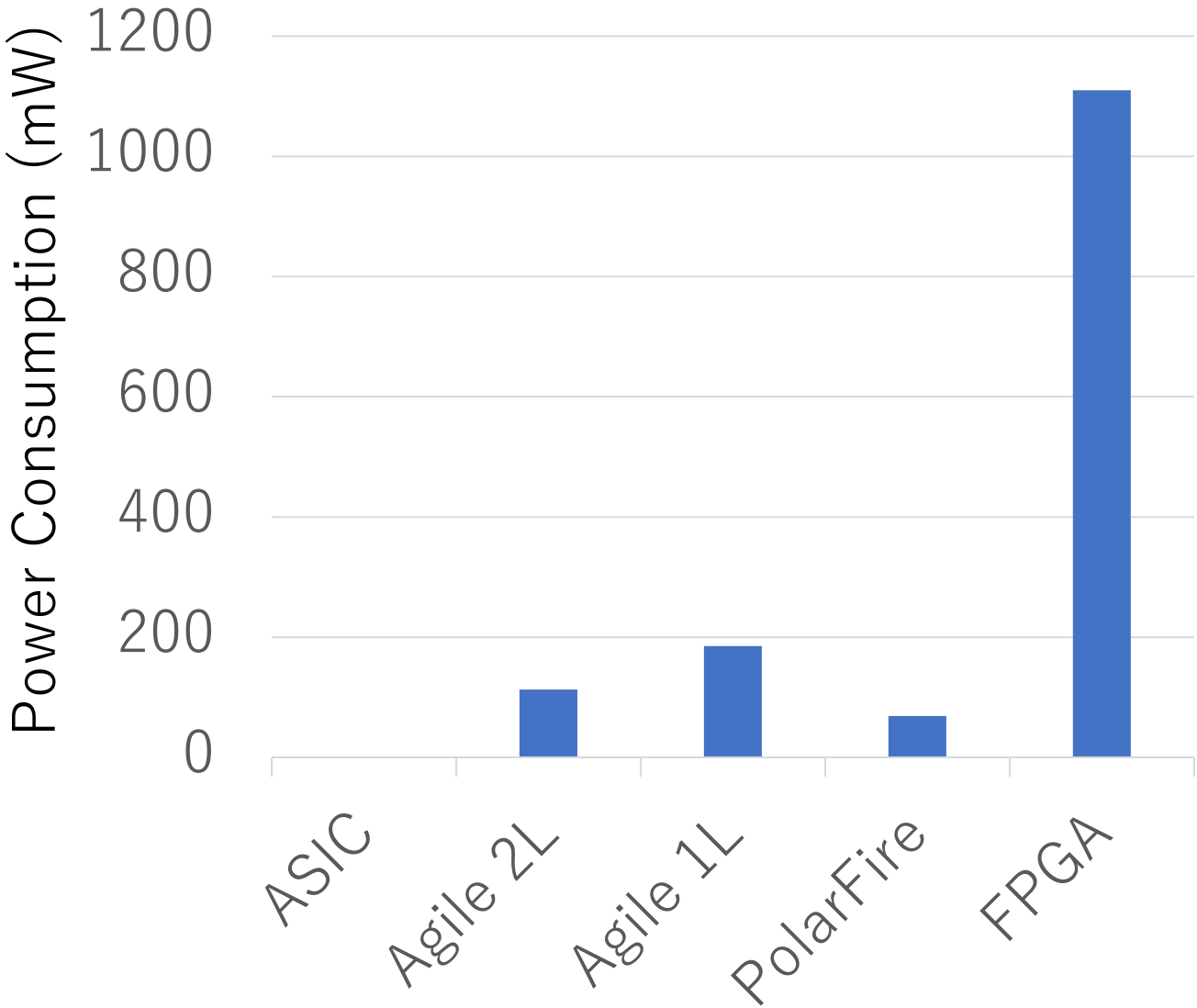
Evaluated Chips and Applications

Evaluated Chips	MPW shuttle (ASIC)	Agile-chip Platform	Polarfile Anti-fuse FPGA	Zunq Ultrascale+ SRAM FPGA
NRE Cost ($)	89.6K	22.2	422	341
Programmability	One-time	One-time	One-time	Many-time
Process (Programming) time	More than 20 days	30 mins	A few mins	a few mins
Process	0.18 μ m 1P6M	0.18 μ m 1P6M	22nm	16nm
Tool	Synopsys Design Compiler 2023.12-SP2	Synopsys Design Compiler 2023.12-SP2	Libero SoC v2024.2 (Service is stopped now)	Vivado 2021.1

Application	
CRC checker	8-bit Cyclic Redundancy Code Checker
DCT	1-dimensional DCT used in JPEG decoder
AES	Advanced Encryption Code 128 encoder
FPC	Frequent Pattern Compression decoder
sXXX	ISCAS benchmark from IWLS 2005

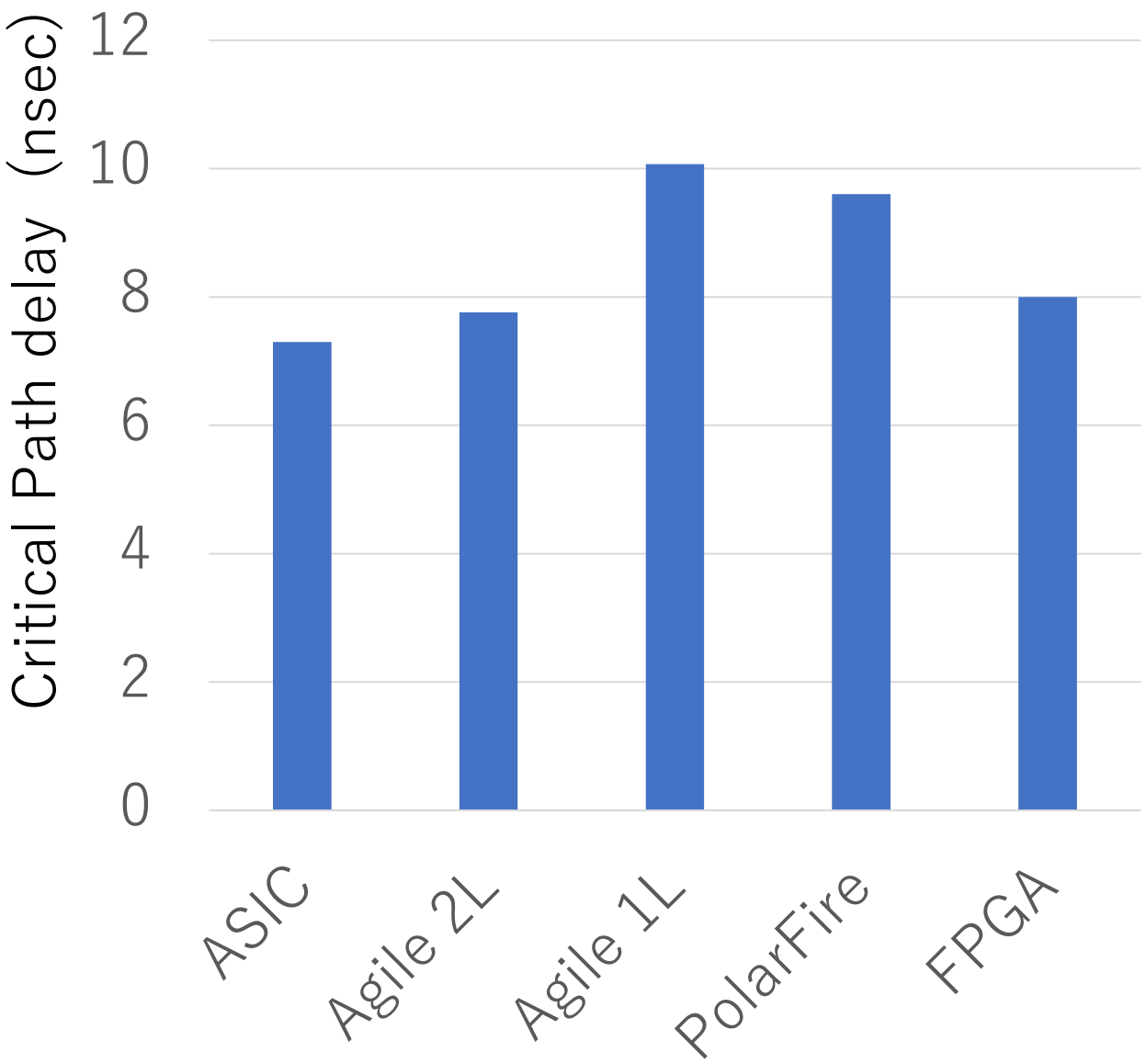
CRC checker

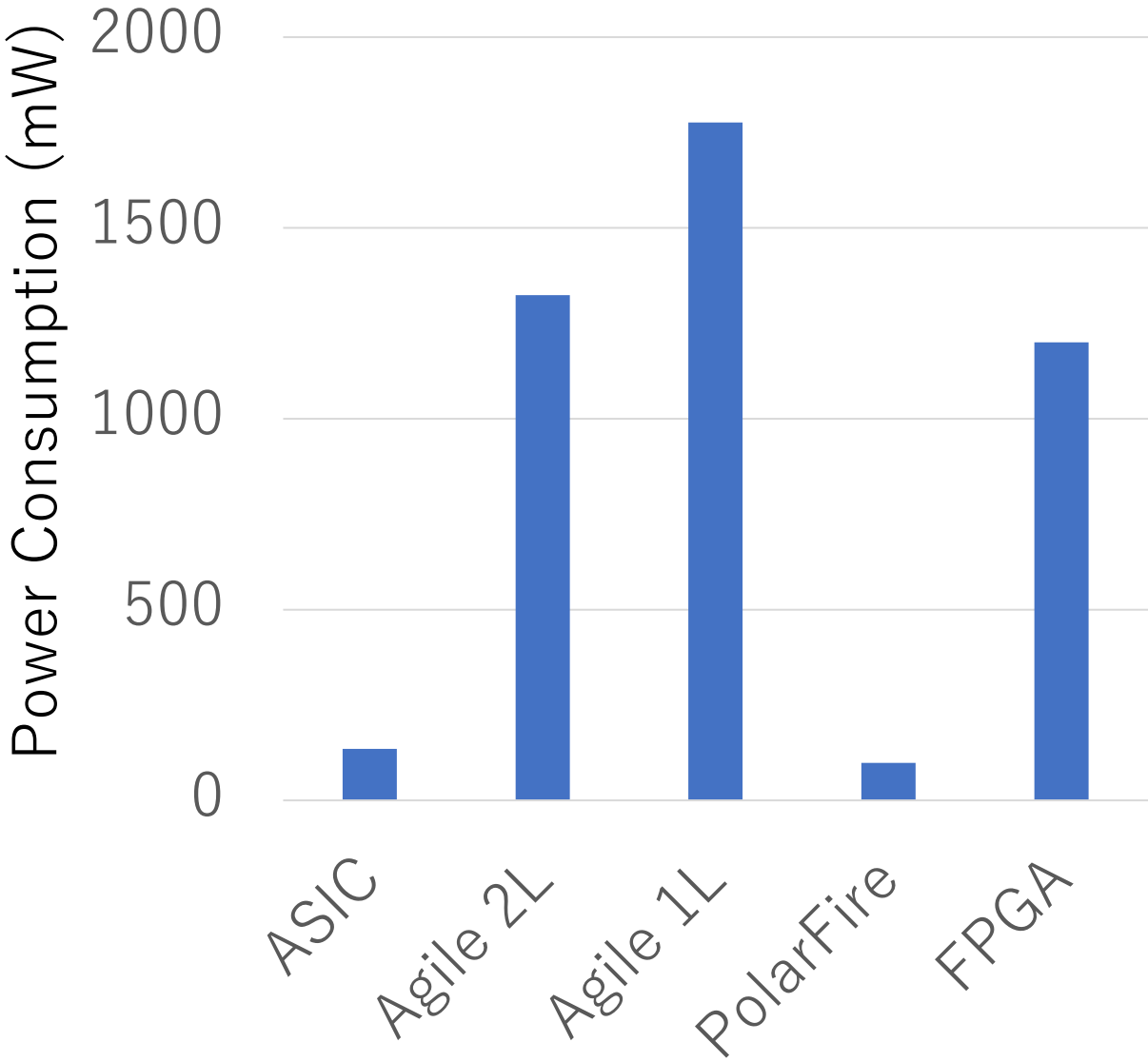




Agile 2L is better than Polarfire and SRAM FPGA in terms of performance.
Polarfire appears to reduce power consumption at the expense of performance.

DCT



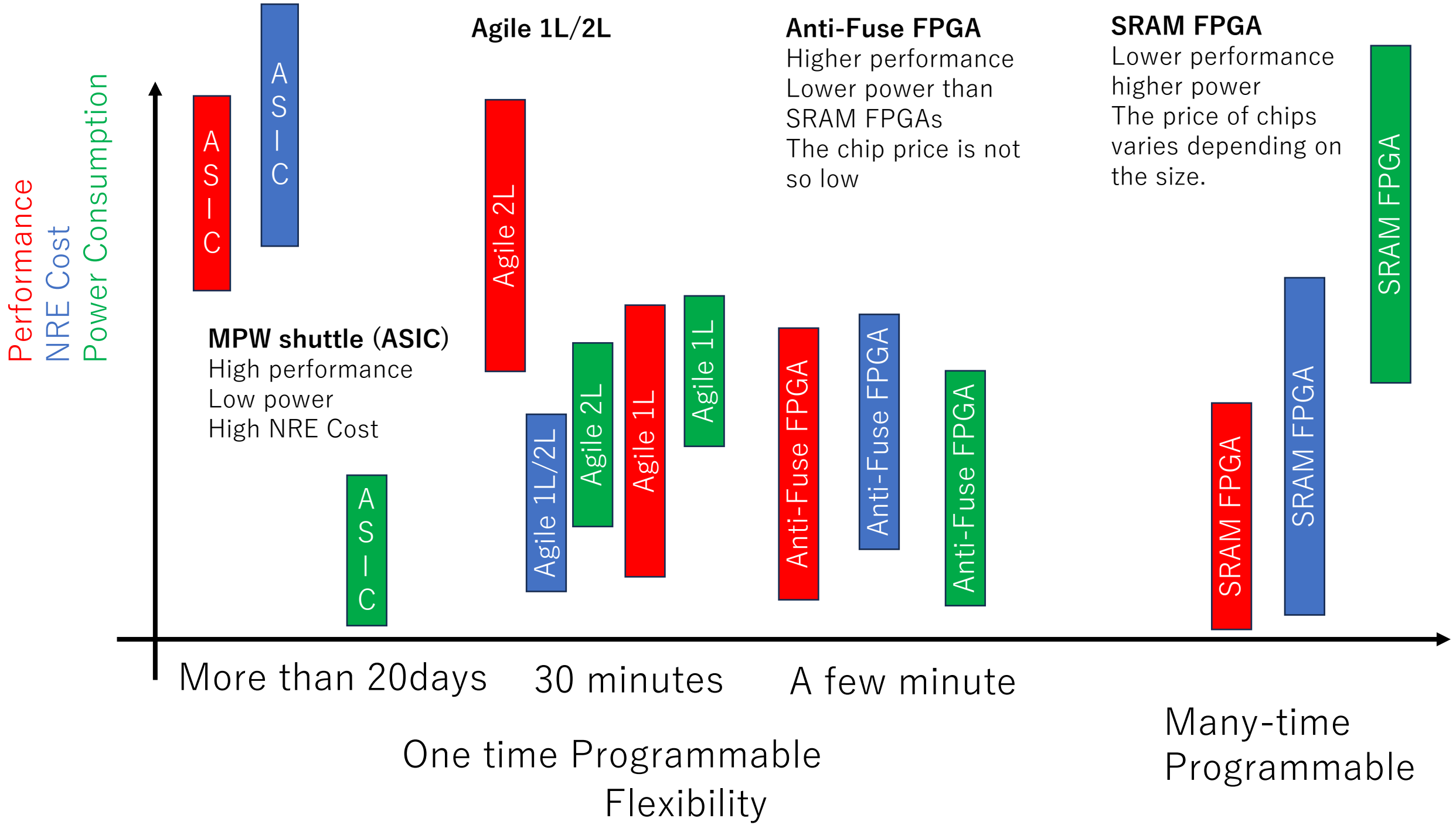


FPGAs with DSP modules are advantageous. Agile 1L is the worst, while Agile 2L is competitive.

Performance and power for other applications

	ASIC	Agile 2L	Agile 1L	FPGA
AES delay(ns)	3.24	4.01	7.27	7.14
power (mW)	59.6	954	910	1166
FPC delay(ns)	3.25	4.51	6.45	4.242
power (mW)	50.8	728	889	1339
s382 delay(ns)	0.3	0.21	0.41	4.84
power (mW)	0.207	22	26	1108
s510 delay(ns)	2.48	3.09	4.45	4.84
power (mW)	0.207	22	26	1113
s820 delay(ns)	2.75	4.89	5.85	4.84
power (mW)	0.113	10.5	16.4	1113

- Polarfire cannot be evaluated because the service has been discontinued.
- The performance of Agile 2L is better than that of FPGA, and close to ASIC.
- The performance of Agile 1L is comparable to FPGA.
- The power of Agile 1L/2L is much better than FPGA, but much worse than ASIC.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Agile 2L
Agile 1L
Agile 1L
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Anti-Fuse FPGA
Anti-Fuse FPGA
SRAM FPGA
SRAM FPGA
More than 20days
30 minutes
A few minute
One time Programmable
Flexibility
Many-time Programmable

Conclusions

- The main advantage of Agile 1L/2L is its low cost for ultra-low-volume production.
- The main issue with Agile 1L/2L at present is the limited number of gates, but this can be improved in the future.
- The performance of Agile 2L is better than FPGAs and close to ASIC.
- The performance of Agile 1L is comparable to that of FPGAs in the application without DSP modules.
- Agile 2L can be used instead of anti-fuse style FPGAs, although Agile 1L is mainly for education.
- Agile chips are advantageous for applications where SRAM-based FPGAs cannot be used, such as operations under high radiation.
- The use of more advanced process is desired.